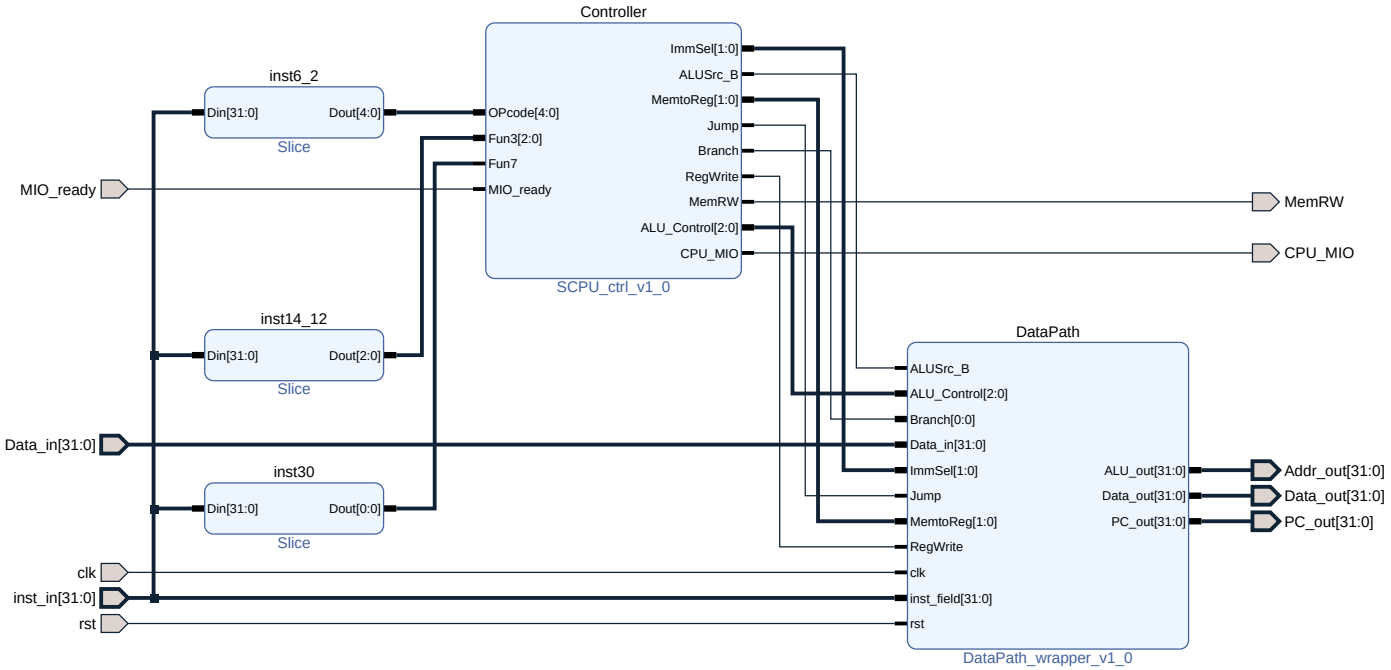
Controller
ImmSel[1:0]
ALUSrc_B
MemtoReg[1:0]
Jump
Branch
RegWrite
MemRW
ALU_Control[2:0]
CPU_MIO
OPcode[4:0]
Fun3[2:0]
Fun7
MIO_ready
SCPU_ctrl_v1_0
inst6_2
Din[31:0]
Dout[4:0]
Slice
inst14_12
Din[31:0]
Dout[2:0]
Slice
inst30
Din[31:0]
Dout[0:0]
Slice
MIO_ready
Data_in[31:0]
clk
inst_in[31:0]
rst
DataPath
ALUSrc_B
ALU_Control[2:0]
Branch[0:0]
Data_in[31:0]
ImmSel[1:0]
Jump
MemtoReg[1:0]
RegWrite
clk
inst_field[31:0]
rst
ALU_out[31:0]
Data_out[31:0]
PC_out[31:0]
DataPath_wrapper_v1_0
MemRW
CPU_MIO
Addr_out[31:0]
Data_out[31:0]
PC_out[31:0]